Amended claims:

5. (Amended) The method of claim 4, wherein the first conductivity type is p type and the second conductivity type is n type.

7. (Amended) A method of providing a device having a holding voltage substantially the same as a conventional GGNMOS, wherein the GGNMOS comprises a n+ drain and a n+ source formed in p-material to define a p-channel between them as provided by any conventional GGNMOS, but supporting current densities that are at least twice as high as for any conventional GGNMOS of substantially the same holding voltage, comprising
providing a SCR-like structure having a p+ emitter, and
sizing the emitter so as to provide a holding voltage of a defined level.

8. A method of providing a device having a holding voltage substantially the same as a conventional GGNMOS , wherein the GGNMOS comprises a n+ drain and a n+ source formed in p-material to define a p-channel between them as provided by any conventional GGNMOS, but supporting current densities that are at least twice as high as for any conventional GGNMOS of substantially the same holding voltage, comprising
providing a LVTSCR-like structure having a p+ emitter and a n+ emitter,
predefining the size of the p+ emitter, and
increasing the size of the n+ emitter to achieve a predefined holding voltage.

9. (Twice Amended) A method of providing a device having a higher holding voltage than a conventional LVTSCR, wherein the LVTSCR includes a n-well in a p-material, with a n+ and a p+ region formed in the p-material, and a second n+ region and a p+ emitter formed in the n-well, and a floating n+ drain formed partly in the n-well and partly in the p-material, and a gate, and supporting a higher current than a conventional GGNMOS, wherein the GGNMOS comprises a n+ drain and a n+ source formed in p-material to define a p-channel between them as provided by any conventional GGNMOS, both made by the same process as the device, comprising providing a LVTSCR-like structure having a p+ emitter that is sufficiently reduced in size relative to a conventional LVTSCR so as to increase the holding voltage to a desired level that is higher than that of a conventional LVTSCR.

11. (Amended) A method of creating an ESD protection structure having a higher holding voltage than a conventional LVTSCR made by the same process, wherein the LVTSCR includes a n-well in a p-material, with a n+ region and a p+ region formed in the p-material, and a second n+ region and a p+ emitter formed in the n-well, and a floating n+ drain formed partly in the n-well and partly in the p-material, and a gate, comprising
providing a LVTSCR-like structure as for the conventional LVTSCR, which includes the p+ emitter, and
manipulating the size of the p+ emitter.

13. A method of creating an ESD protection structure that supports a higher current than a conventional GGNMOS device made by the same process as the structure, , wherein the GGNMOS comprises a n+ drain and a n+ source formed in p-material to define a p-channel between them as provided by any conventional GGNMOS, comprising

providing a LVTSCR-like structure which includes a n-well in a p-material, with a n+ region and a p+ region formed in the p-material, and a second n+ region and a p+ emitter formed in the n-well, and a floating n+ drain formed partly in the n-well and partly in the p-material, and a gate, p+ emitter, and

manipulating the size of the p+ emitter.

15. A method of varying the holding voltage of a LVTSCR, which includes a p+ emitter and a n+ emitter, comprising

adjusting the size of the p+ emitter.